Patent Claims

1. A memory module (1) comprising:

- a carrier substrate (50) having terminals (40) for supplying address and command signals (ADR, CMD),

- a plurality of integrated memory components (10 to 18, 20 to 28) which are arranged on the carrier substrate,

- an access control circuit (30), which is arranged separately from the memory components on the carrier substrate, is connected, on the input side, to the terminals (40) for supplying the address and command signals and is connected, on the output side, to the plurality of integrated memory components (10 to 18, 20 to 28),

- the access control circuit (30) being designed in such a manner that, when supplying an address signal (ADR) which has been generated outside the memory module, it receives an address for a memory access to a memory component which has been selected for the access, respectively generates, from the address received, at least one column address (CADR) and one row address (RADR) for the purpose of accessing a bit line (BL) and a word line (WL) of the selected memory component and transmits said addresses to the selected memory component.

2. The memory module as claimed in claim 1,

wherein

the access control circuit (30) is furthermore designed in such a manner that, when supplying an access command (R/W) which has been generated outside the memory

module (1) and indicates the beginning of a memory access, it receives said command and generates therefrom an access signal sequence having at least one activation signal (ACT) and a subsequent read or write signal (RD, WR) for transmission to the selected memory component.

3. The memory module as claimed in claim 1 or 2,

wherein

the column address (CADR) and row address (RADR) for accessing a bit line (BL) and word line (WL) are generated successively in time by the access control circuit (30) for transmission to the selected memory component.

4. The memory module as claimed in claim 3,

wherein

the column address (CADR) and row address (RADR) for accessing a bit line (BL) and word line (WL) are generated by the access control circuit (30) in such a manner that they are offset by an RAS-CAS delay time, the latter being defined by the selected memory component.

5. The memory module as claimed in one of claims 1 to 4,

wherein

the access control circuit (30) is arranged within a separate semiconductor module.

6. The memory module as claimed in one of claims 1 to 5,

wherein

the input-side terminal of the access control circuit (30) is connected to a contact strip (40) of the memory module (1).

7. The memory module as claimed in one of claims 1 to 6,

wherein

the memory module (1) is in the form of a DIMM module arrangement.

8. The memory module as claimed in one of claims 1 to 7,

wherein

the memory components (10 to 18, 20 to 28) of the memory module (1) are dynamic random access memories.